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Superscalar pipelined inner product computation unit for signed unsigned number☆

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Summary In this paper, we proposed superscalar pipelined inner product computation unit for signed-unsigned number operating at 16 GHz. This is designed using five stage pipelined operation with four 8×8 multipliers operating in parallel. Superscalar pipelined is designed to compute four 8×8 products in parallel in three clock cycles. In the fourth clock cycle of the pipeline operation, two inner products are computed using two adders in parallel. Fifth stage of the pipeline is designed to compute the final product by adding two inner partial products. Upon the pipeline is filled up, every clock cycle the new product of 16×16-bit signed unsigned number is obtained. The worst delay measured among the pipeline stage is 0.062 ns, and this delay is considered as the clock cycle period. With the delay of 0.062 ns clock cycle period, the pipeline stage can be operated with 16 GHz synchronous clock signal. Each superscalar pipeline stage is implemented using 45 nm CMOS process technology, and the comparison of results shows that the delay is decreased by 38%, area is reduced by 45% and power dissipation is saved by 32%.

Introduction

The dedicated vector processors, supercomputers, and the modern digital signal processors have the multiple pipeline units. In these multiple pipeline units, the multiplier operation is the most time critical operation. Hence, we proposed five stage superscalar pipelined inner product computation unit for high performance, small chip area, and lower power consumption. In superscalar pipeline technique, multiple instructions and arithmetic operations are executed in parallel and overlapping. The multiple, the parallel and the pipeline concept can enhance the performance of the system. Our proposed superscalar pipeline uses four 8-bit multipliers in parallel and pipeline for the computation of product of 16×16-bit signed unsigned number.

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To address the need of very high speed modern processors (Hong et al., 2006; Alshawi et al., 2015; Olivieri, 2001; Lin, 2001; Hoyer et al., 2001; Jou et al., 1997) illustrated the design of multipliers. In Hong et al. (2006) and Alshawi et al. (2015) illustrated the design of very high speed matrix multiplier matrix, but without using the pipeline technique. In Olivieri (2001) illustrated the pipeline of the Carry Save Adder (CSA) for the partial product reduction tree (PPRT) and not all the stages, therefore the selection of high speed clock signal is difficult. In Lin (2001) illustrated an array of 8×8 or 4×4 multiplier for the inner product computation, with high speed, small area, and lower power dissipation. But this paper fails to address the number of pipeline stages. In Hoyer et al. (2001) illustrated the micro-pipelines using asynchronous local clock signal, but in this pipelined operation is not regular. In Hong et al. (2006), Alshawi et al. (2015), Olivieri (2001), Lin (2001), Hoyer et al. (2001) and Jou et al. (1997) have used Modified Booth Encoder (MBE) technique as partial product generator (PPG), and Shin et al. (2010), Yeh and Jen (2000), Kuang et al. (2009) and Wang et al. (2008) presented the design of MBE with different number of transistors. The second phase in the multiplier is to convert n rows of partial product into two rows called as PPRT illustrated in Wang et al. (2008), Goto et al. (1997), Chang et al. (2004), Radhakrishnan and Preethy (2000) and Prasad and Parhi (2001). Finally, the concept of high speed carry propagate adder (CPA) such as Carry Look-Ahead (CLA) adder is illustrated in Oklobdzija et al. (1996), Kim and Ambler (2000), Zlatanovici et al. (2009), Nagendra et al. (1996), Wang et al. (2002), Lee et al. (2001), Kim et al. (2002) and Nève et al. (2004).

Design of inner product superscalar pipeline multiplier

Fig. 1 shows the architecture of inner product computation unit, which consists of 4 multipliers operating in parallel for the 16×16-bit multiplication. The 16-bit word length of operand (A) and operand (B) is decomposed into $w = 8$-bit MSBs and 8-bit LSBs, and the four 8-bit multipliers computes the product in parallel as given by Eq. (1). The five stages of the superscalar pipelined multiplier consist of generating partial products, compression of an array of five rows into an array of two rows. Remaining three high speed adder stages is used to obtain the product. The five stage of the superscalar pipeline multiplier is illustrated in the following section.

$$A \times B = A_{8LSB} \times B_{8LSB} + (A_{8MSB} \times B_{8LSB})2^{w} + (A_{8LSB} \times B_{8MSB})2^{w} + (A_{8MSB} \times B_{8MSB})2^{2w} \quad (1)$$

Superscalar pipeline stage 1: four partial product generator in parallel

The superscalar pipeline stage 1 comprises of four PPG as illustrated in Fig. 2. The PPG accepts operands a_7–a_0, a_{15}–a_8, b_7–b_0, and b_{15}–b_8 simultaneously during the first stage of the superscalar pipeline operation. The PPG using multiplexer based MBE (MMBE) is implemented using 16

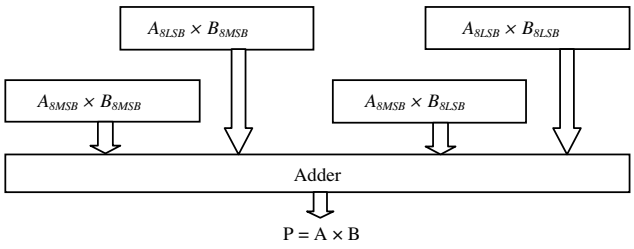

Figure 1 Architecture of inner product computation.

$$\begin{array}{r} a_7\,a_6\,a_5\,a_4\,a_3\,a_2\,a_1a_0 \\ b_7b_6\,b_5\,b_4\,b_3\,b_2\,b_1\,b_0 \\ \hline \overline{p_{08}}\,p_{08}\,p_{08}\,p_{07}\,p_{06}\,p_{05}\,p_{04}\,p_{03}\,p_{02}\,p_{01}\,p_{00} \\ 1\;\; p_{18}\,\overline{p_{17}}\,p_{16}\,p_{15}\,p_{14}\,p_{13}\,p_{12}\,p_{11}\,p_{10} \quad n_0 \\ 1\;\; p_{28}\,\overline{p_{27}}\;\; p_{26}\,p_{25}\,p_{24}\,p_{23}\,p_{22}\,p_{21}\,p_{20} \quad n_1 \\ 1\;\; \overline{p_{38}}\;\; p_{37}\;\; p_{36}\;\; p_{35}\;\; p_{34}\;\; p_{33}\,p_{32}\;\; p_{31}\,p_{30} \quad n_2 \\ C_{47}\,p_{46}\;\; p_{45}\;\; p_{44}\;\; p_{43}\;\; p_{42}\;\; p_{41}\,p_{40} \quad n_3 \\ \hline p_{15}\;\; p_{14}\,p_{13}\;\; p_{12}\;\; p_{11}\;\; p_{10}\;\; p_9\;\; p_8\;\; p_7\;\; p_6\;\; p_5\;\; p_4\;\; p_3\;\; p_2\;\; p_1\;\; p_0 \end{array}$$

Figure 2 8×8 multiplier for signed and unsigned numbers.

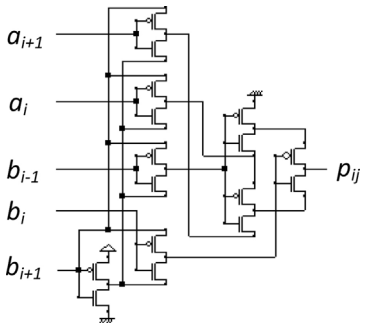

Figure 3 Circuit diagram of MMBE.

transistors as shown in Fig. 3. The MMBE taking three bits of multiplier operand simultaneously produces five partial products. Since the superscalar multiplier is to function for signed ($s\_u = 1$) and unsigned ($s\_u = 0$) number, the requirement of the sign extend logic is given by the following expression.

$s\_u = 1,\ a_{n-1} = 1,\ b_{n-1} = 0,\ a_n = a_{n+1} = 1$ and $b_n = b_{n+1} = 0$

$s\_u = 1,\ a_{n-1} = 0,\ b_{n-1} = 1,\ a_n = a_{n+1} = 0$ and $b_n = b_{n+1} = 1$

$s\_u = 0,\ a_n = a_{n+1} = 0$ and $b_n = b_{n+1} = 0$

$C_{ij} = s\_\bar{u}a_{n-1}a_{n-2}$

Superscalar pipeline stage 2: PPRT as 5:2 compressors

During the second stage of the superscalar pipeline, five partial products of the stage 1 is accepted by four PPRT and reduced to an array of two rows and latch into the registers using synchronous clock signal. The Vertical Column Adder (VCA) functions as PPRT and converts five rows into two rows. In Goto et al. (1997), Chang et al. (2004), Radhakrishnan and Preethy (2000) and Prasad and Parhi (2001) the PPRT consists of full adders only, but VCA consists of full adders and the Sum Carry Generate and Propagate (SCGP) logic. The SCGP logic circuit produces the Sum, Carry Generate term and the Carry Propagate term, which are essential for the CLA operation. The design of high performance full adder is implemented using Eqs. (2) through (3).

$$s_i = x_{i+1} \oplus x_{i+2} \oplus c_i \tag{2}$$

$$c_{i+1} = (x_{i+1} \oplus x_{i+2})c_i + \overline{(x_{i+1} \oplus x_{i+2})}x_{i+1} \tag{3}$$

The circuit diagram of full adder is shown in Fig. 4. This is implemented in CMOS logic using only ten transistors. The required logic for SCGP is derived from Eq. (3) as given by Eqs. (4) and (5). Where cp_i is called carry propagate term, and cg_i is called carry generate term. Fig. 5 shows the circuit diagram of SCGP logic, this is the final cell of each VCA. This is designed to perform operations such as sum, carry generate and carry propagate terms to save the extra hardware for carry generate and carry propagate terms and is implemented in CMOS logic using only ten transistors.

$$cp_i = x_{i+1} \oplus x_{i+2} \tag{4}$$

$$cg_i = \overline{(x_{i+1} \oplus x_{i+2})}x_{i+1} \tag{5}$$

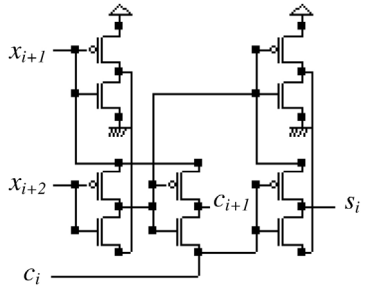

Figure 4 Circuit diagram of full adder.

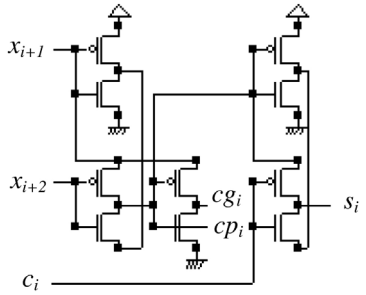

Figure 5 Circuit diagram of SCGP.

Superscalar pipeline stage 3: computation of 8 × 8 inner product in parallel

During the third stage of superscalar pipeline, the final two rows from the PPRT is added using four CPA to obtain the products of four 8 × 8 multipliers in parallel. The CPA which combines the effect of Carry Look-ahead Adder and Carry Select Adder (CLCSA) is as shown in Fig. 6. In CLCSA, all the 8-bit CLA adders produce carry in parallel with two such 8-bit CLA's in each stage with 0 and 1 as the initial carry input. Depending on the carry output generated from the previous stage of 8 bit CLA, the output selected by the 2:1 multiplexer is the carry signal to the next stage. Thus the CLCSA generates carry in parallel and the final product with high performance.

Pipeline stage 4: inner partial product computation

The four 8 × 8 products obtained from the pipeline stage 3 are k_{15}–k_0, l_{15}–l_0, m_{15}–m_0, and n_{15}–n_0. During the pipeline stage 4, these four partial products are added using two 24-bit adders in parallel as shown in Fig. 2. The CLCSA of Fig. 6 is extended for the addition of 24-bit operands by including a set 8-bit CLA adder and a 2:1 eight multiplexers. Two CLCSA adders operating in parallel can produce two inner partial products x_{24}–x_0 and y_{24}–y_0. And these two inner products are latched into the register using the synchronous clock signal. The delay measured for the pipeline stage 4 is 0.051 ns. Thus, the superscalar pipeline stage 4, requires four 16-bit operands every pipeline clock cycle of 16 GHz to produce two 25-bit inner product in parallel.

Pipeline stage 5: final product computation

During the pipeline stage 5, the final two inner partial products obtained from the stage 4 are added in parallel to obtain the product of 16 × 16-bit multiplier. The CLCSA of Fig. 6 can be used to add 32-bit inner products x and y to obtain the product of 16 × 16-bit multiplier. The CLCSA of Fig. 6 is extended for the addition of 32-bit operands by including two sets of 8-bit CLA adder and two sets of 2:1 eight multiplexers. The 32-bit CLCSA adder produces 32-bit product, and is latched into the register using the synchronous clock signal. The delay measured for the pipeline stage 5 is 0.062 ns, and is operated with the clock frequency of 16 GHz. The pipeline fills up in the 5th clock cycle, once the pipelined is filled up, every clock cycle the new product of 16 × 16-bit multiplier is generated. Superscalar pipeline requires two 16-bit operands every pipeline clock cycle of 16 GHz to produce the product of 16 × 16-bit signed unsigned multiplier.

Experimental results

For comparison, we have implemented several pipelined multipliers. Each pipeline multiplier is divided into five stages. The five stages of the pipeline multiplier are the PPG, PPRT, and three CPA. Each pipeline stage is implemented using the digital schematic, and the Verilog HDL code is

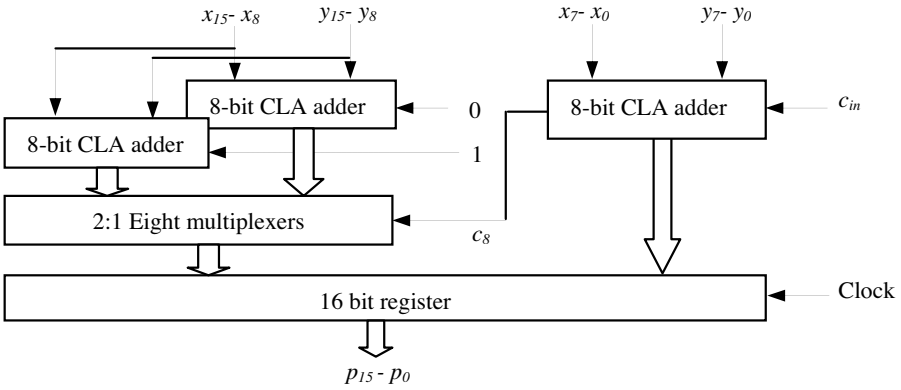

Figure 6 Architecture of CLCSA for 8 × 8-bit multiplier.

Table 1 Comparison of multipliers.

Multiplier size	References	Number of transistors	Cycle time (ns)	Area (μm^2)	Power (mW)	Clock frequency (GHz)
16 × 16	Hong et al. (2006)	34,620	0.085	3093.28	605.8	11.0
	Alshawi et al. (2015)	34,846	0.075	2646.00	680.8	13.0
	Hoyer et al. (2001)	32,472	0.097	2580.48	518.4	10.0
	Proposed	18,468	0.062	1679.60	477.0	16.0

obtained by compiling the digital schematic. Then the Verilog HDL code is compiled to obtain the layout using the 45 nm CMOS technology Microwind Tool. Finally, the layout is synthesized and measured the critical path delay, the area, and the power consumption. For the pipelined multiplier, the maximum critical path delay of the pipeline stage is considered as the clock cycle. That is the maximum delay of PPG, PPRT and CPA. The maximum delay (0.023 ns, 0.046 ns, 0.056 ns, 0.062 ns) is 0062 ns. Therefore, the delay 0.062 ns is considered as the pipeline clock cycle, and the pipeline stage is operated with the frequency (f) = 1/0.062 = 16 GHz. Also the area and power measured is listed in Table 1. Comparison of results shows that our proposed three stage pipeline multiplier has been improved in delay by 38%, area reduced by 45% and power dissipation saved by 32%.

Conclusion

The superscalar pipeline multiplier is operated with two 16-bit operands in parallel, and the operands are decomposed into four 8-bit operands. With four operands in parallel, at the end of the third stage inner product is also computed in parallel. And using the CPA at three levels the final 16 × 16-bit product of signed unsigned number is obtained. The superscalar pipeline fills up in five clock cycles, and there after every clock cycle 16 × 16-bit product is generated. Finally, the comparison of results shows that our proposed five stage superscalar pipeline multiplier, improved in delay by 38%, area reduced by 45% and power dissipation saved by 32% and operates 16 GHz clock signal frequency.

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